R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, in FIG. 1, as originally filed. Thus, no new matter has been added.

OBJECTION TO THE SPECIFICATION

Objection to the specification is respectfully traversed and should be withdrawn. Applicants' representative is unable to identify the "several minor typographical errors" allegedly found in the specification. The Examiner is respectfully requested to either (i) identify each alleged problem or (ii) withdraw the rejection.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-14, 17-19, 22-26 and 29-31 under 35 U.S.C. §103(a) as being unpatentable over Narayana et al. '920 (hereafter Narayana 1) in view of Narayana et al. '897 (hereafter Narayana 2) is respectfully traversed and should be withdrawn.

The rejection of claims 15, 16, 20 and 21 under 35 U.S.C. §103 as being unpatentable over Narayana 1 and Narayana 2 in view of Andrews '314 is respectfully traversed and should be withdrawn.

Narayana 1 concerns a half-full flag generator for synchronous FIFOs (Title). Narayana 2 concerns a signal generation decoder circuit and method (Title). Andrews concerns programmable timing circuit for integrated circuit device with test access port (Title).

Claim 1 provides a state machine configured to generate an output signal in response to a first programmable almost full look-ahead signal and a second programmable almost full look-ahead signal. In contrast, the Office Action has not established that a signal 22 (asserted similar to the claimed first programmable almost fill look-ahead signal) and a signal 34 (asserted similar to the claimed second almost full look-ahead signal) of Narayana 1 are both (i) programmable and (i) almost full signals. Therefore, *prima facie* obviousness has not been established.

Furthermore, the assertion page 3 of the Office Action that "Narayana '897 teaches a state machine indicating a fullness of a FIFO similar to that of Narayana '920" appears to be a conclusory statement. In particular, no evidence is provided in the Office Action that the state machines of Narayana 1 and Narayana 2 are similar. Therefore, *prima facie* obviousness has not been established.

Furthermore, clear and particular motivation to combine the references has not been established. The asserted motivations on page 3 of the Office Action (i) "so that the almost-fullness of the FIFO could be determined" and (ii) "the almost-full state machine means taught by Narayana '897 would improve the flexibility of Narayana '920" are not credited to either reference or knowledge generally available to one or ordinary skill in the art as required by MPEP §2142. Therefore, the asserted motivations appear to be conclusory statements. As such, *prima facie* obviousness has not been established and the rejection of claim 1 should be withdrawn.

Claim 2 provides a synchronizer configured to generate a synchronized output signal in response to a second set-output signal (generated by a second set state machine) and a reset signal. In contrast, page 4 of the Office Action asserts that a block 14 of Narayana 1 generates a signal 32 similar to the claimed second set-output signal and an SR latch 19 of Narayana 1 is similar to the claimed synchronizer. However, the SR latch 19 of Narayana 1 does not appear to receive the signal 32. Therefore, *prima facie* obviousness has not been established.

Claim 2 further provides a latch configured to generate a first latch output signal in response to a first set-output signal (generated by a first set state machine) and the synchronized output signal. In contrast, page 4 of the Office Action asserts that a block 16 of Narayana 1 is similar to the

claimed latch. However, the block 16 of Narayana 1 does not appear to respond to a signal generated by the SR Latch 19 (asserted similar to the claimed synchronizer). Therefore, *prima facie* obviousness has not been established.

Claim 2 further provides a first logic block configured to generate a first control signal (used by a first set state machine) in response to a second latch output signal (generated by the latch). In contrast, page 4 of the Office Action asserts that a block 15 of Narayana 1 is similar to the claimed first logic block. However, the output of block 15 of Narayana 1 does not appear to be received by the block 11 (asserted similar to the claimed first set state machine). Therefore, *prima facie* obviousness has not been established.

Claim 2 further provides a second logic block configured to generate (i) the reset signal (used by the synchronizer) and (ii) a second control signal (used by a second set state machine) in response to the first latch output signal. In contrast, page 4 of the Office Action asserts that a block 18 of Narayana 1 is similar to the claimed second logic block. However, (i) the block 18 of Narayana 1 does not appear to generate two signals as claimed and (ii) the only signal generated by the block 18 does not appear to be received by either the SR Latch 19 (asserted similar to the claimed synchronizer) or the block 14 (asserted similar to the

claimed second set state machine). Therefore, *prima facie* obviousness has not been established.

Furthermore, the Office Action makes no assertion that Narayana 1 could be combined with Narayana 2 to account for the above differences between the claimed structure and the asserted similarities. Claim 29 provides language similar to claim 2. As such, the rejections of claims 2 and 29 should be withdrawn.

Claim 22 provides a method for determining an almost emptiness of at least one memory buffer. The Office Action admits on page 8 that neither Narayana 1 or Narayana 2 alone, teaches or suggests all of the claimed steps. The Office Action provides no clear and particular evidence of motivation to combine the references. The Office Action provides no evidence that a combination of the references would teach or suggest all of the claimed steps. Therefore, *prima facie* obviousness has not been established. As such, the rejection of claim 22 should be withdrawn.

Claim 3 provides a synchronizer and a SR latch. In contrast, page 5 of the Office Action asserts that a block 19 of Narayana 1 is similar to both the claimed synchronizer and the claimed SR latch. Since a single element in a reference does not teach or suggest a claimed structure having two elements, *prima facie* obviousness has not been established. The arguments in the Office Action for rejecting claims 10 and 11 have similar problems

where a single element in Narayana 1 is asserted similar to two claimed elements. As such, the rejections for claims 3, 10 and 11 should be withdrawn.

Regarding claims 15, 16, 20 and 21, clear and particular evidence of motivation to combine Narayana 1 and Narayana 2 with Andrews has not been established. In particular, the asserted motivations on page 10 of the Office Action (i) "to ensure reliable timing adjustments to compensate for clock skew" and (ii) " because it allowed for reliable timing without the need of separate set of test instrumentation" do not appear to be based on column 1, lines 25-40 and column 1, lines 54-67 of Andrews as alleged. The cited text of Andrews reads:

> The calibration and tuning of system timing provided by a system timing generator circuit is a critical factor in system performance including memory performance. Increasing clock frequencies require less skew between related signals while timing measurement becomes more difficult. Both factory calibration and field tuning may be unsatisfactory for a subsequent user. Inexperienced technicians may also misadjust timing during factory or field tuning.
>
> Failure of system timing is also due to the use of discrete wire wound delay line components packaged in separate dual-in-line packages (DIPs). Such discrete delay lines are unreliable and a major cause of system failure. Other timing calibration tools such as monostable multi-vibrators and decoded counters suffer from drift and low resolution.
>
> ...
>
> The test access port (TAP) defined by IEEE Standard 1149.1 Test Access Port and JTAG Version 2.0 for incorporation on an integrated circuit chip is illustrated in FIG. 1. At least four pins of the IC device and up to 3% to 25% of the chip silicon surface area is dedicated to the test access port and associated TAP circuits. The TAP is intended to standardize and facilitate boundary scan testing and other design specific testing of the IC device while the chip is

> still mounted on a circuit board and without separate test instrumentation. The TAP permits all phases of testing with access at all pins of the IC device through boundary scan principles even for surface mount devices and without the necessity of "bed of nails" physical contact. Access to all pins for testing is achieved electronically through the boundary scan shift register, one of the test data registers of the test access port.

Nowhere in the above text does Andrews appear to mention (i) ensuring reliable timing adjustments or (ii) allowing for reliable timing without separate test instruments. Therefore, the asserted motivations appear to be merely conclusory statements. As such, *prima facie* obviousness has not been established.

Furthermore, Andrews appears to be non-analogous art with respect to Narayana 1 and Narayana 2 based on differences in the US Classifications. The Examiner has also failed to established that Andrews, Narayana 1 and Narayana 2 are either in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned (MPEP 2141.01(a)). Therefore, *prima facie* obviousness has not been established. As such, the rejections for claims 15, 16, 20 and 21 should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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